REMARKS

Claims 1-3, 5-7, 9-11, 13-19, 21-26, 28-32 and 34-36 remain pending in the Application. No new matter has been added. Applicants respectfully request reconsideration in view of the following remarks.

I. Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claims 1-3, 5-7, 9-11, 13-19, 21-26, 28-32 and 34-36 as allegedly unpatentable over U.S. Patent No. 6,738,248 ("Jenkins") in view of U.S. Patent No. 5,994,760 ("Duclos") and International Publication No. WO 02/05380 A1 ("Rutfors"). Applicants respectfully traverse this rejection.

a. Claim 1 and its dependent claims

Claim 1 is directed to a low noise amplifier that includes a radio frequency input and an electrostatic discharge ("ESD") protection circuit to shunt ESD current during positive and negative ESD events away from the radio frequency input and through a first supply. The ESD protection circuit includes a pair of diodes and a separate ESD clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an ESD event. The first diode of the pair has a first terminal coupled to the radio frequency input and a second terminal directly coupled to a first supply. The second diode of the pair has a second terminal coupled to the radio frequency input and a first terminal directly coupled to the first supply.

The Examiner suggests that Jenkins' protection circuit 108 is Applicants' claimed electrostatic discharge protection circuit. The Examiner acknowledges that Jenkins does not teach Applicants' claimed separate electrostatic discharge clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an electrostatic discharge event. However, the Examiner suggests that Fig. 2 of Duclos shows this ESD clamp. The Examiner suggests that it would have been obvious to incorporate Duclos' clamp into Jenkins' design "for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply." Applicants respectfully disagree.

Jenkins shows a protection circuit 108 that protects a differential input buffer 102 during ESD events. (Col. 3, lines 6-10). Jenkins discloses three different embodiments of the

protection circuit. In a first embodiment, the protection circuit includes two back-to-back diode pairs coupled between differential inputs to the buffer and a negative voltage supply VSS. (Fig. 1; Col. 3, lines 16-20). In response to an ESD event, one or more of the diodes turns on and discharges the ESD current directly to the VSS supply rail. (Col. 3, lines 43-53). In a second embodiment, the diode pairs are coupled between the buffer inputs and a positive voltage supply VDD, and ESD current is discharged to the VDD rail. (Fig. 2; col. 4, lines 6-11). In a third embodiment of the protection circuit, a diode pair is coupled between the input and an intermediate node 304. (Fig. 3; Col. 4, lines 35-39). Over-voltages at the input are discharged to the VDD and VSS supply rails by diodes D5 and D6, respectively. (Col. 4, lines 39-45). D5 and D6 serve as a voltage clamp, maintaining the voltage between VSS and VDD at about 1.4V. (Id.).

Applicants respectfully assert that the Examiner has not carried his burden of establishing a *prima facie* case of obviousness, because he has not shown a valid motivation to combine Jenkins and Duclos. The Examiner states that it would have been obvious to modify Jenkins' design by incorporating Duclos' clamp between Jenkins' VDD and VSS terminals "for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply." However, as Applicants explained in the response to the previous Office Action, Jenkins already provides a way to protect the buffer 102 from ESD events occurring at the supply: the embodiment of Fig. 3, in which ESD events occurring at the supply are discharged through the direct path formed by diodes D5 and D6. (Fig. 3). Jenkins does not contain any suggestion or motivation to modify the protection circuit to include Duclos' clamp – rather, Jenkins teaches away from adding Duclos' clamp because Jenkins already discloses a way to protect the buffer 102 from ESD events occurring at the supply.

Not only does Jenkins already disclose this protection circuit for ESD events occurring at the supply, Jenkins' protection circuit uses a clamp configuration: diodes D5 and D6 clamp the voltage between VDD and VSS to about 1.4V. (Col. 4, lines 44-45). Certainly, Jenkins cannot be read to include a suggestion to modify its existing clamp protection circuit in order to incorporate yet another clamp protection circuit (i.e., the circuit of Duclos' Fig. 2). Combining Jenkins and Duclos would only duplicate Jenkins' existing protection efforts.

The Examiner responds to these arguments by noting that Jenkins' third embodiment (showing the ESD protection clamp for ESD events at the supply) was not the embodiment that he relied on to reject claim 1. Applicants respectfully submit that this is irrelevant to Applicants' point. The Examiner's stated motivation to combine Jenkins with Duclos is to provide "protection to the buffer (102) from ESD occurring at the power supply." Jenkins already discloses a way to provide protection to the buffer 102 from ESD occurring at the power supply – namely, by using a clamp circuit of the configuration shown in Fig. 3. This disclosure defeats any contention that a suggestion exists to modify Jenkins design to include Duclos' ESD clamp.

The Examiner further states that although Jenkins' Fig. 3 "discloses a method of ESD protection from power line to power line, it does not provide bi-directional ESD protection." Applicants respectfully assert that it is immaterial whether Jenkins could have chosen a *better* way to provide ESD protection to the buffer (e.g., bi-directionally), such as by using Applicants' claimed configuration – the fact remains that Jenkins already discloses *three different* protection circuits for protecting the input buffer, one of which uses a clamp configuration. It is improper to use hindsight to combine features from different references unless those references display a motivation to combine. *See, e.g., In re Dance*, 160 F.3d 1339, 1343 ("obviousness cannot be established by hindsight combination to produce the claimed invention... it is the prior art itself, and not the applicant's achievement, that must establish the obviousness of the combination") (Fed. Cir. 1998). Jenkins clearly knew about Duclos' back-to-back diode configuration – see, for example, Jenkins' back-to-back diode protection circuit shown in Fig. 1 – and, for protection from ESD events at the supply, chose instead to use the clamp configuration shown in Fig. 3. Moreover, as claim 1 does not recite a "bi-directional" limitation, the presence or absence of any such feature in the alleged prior art is immaterial. For at least these reasons, Applicants respectfully assert that the Examiner has not carried his burden of establishing a *prima facie* case of obviousness, and therefore claim 1 is allowable.

The Examiner further acknowledges that Jenkins does not teach that the input is a radio frequency input. The Examiner suggests that Rutfors shows this limitation and that it would have obvious to combine the teachings of Jenkins and Rutfors "for the purpose of providing ESD protection to a wireless circuit thus preventing the [low noise amplifier] from being damaged."

Again, Applicants respectfully submit that the Examiner has not carried his burden of establishing a motivation to combine Jenkins with Rutfors. It is insufficient to merely state the advantages of a particular limitation, i.e., to merely note that adding ESD protection would be desirable to prevent damage to an amplifier. The fact that references can be combined is insufficient to establish a *prima facie* case of obviousness - rather, the Examiner must point to a suggestion that this modification must be made. *See, e.g., In re Gorman*, 933 F.2d 982, 987 (Fed. Cir. 1991) ("It is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant's structure as a template and selecting elements from references to fill the gaps.... The references themselves must provide some teaching whereby the applicant's combination would have been obvious.") The Examiner has cited to no such suggestion in Rutfors or in the art, and indeed, there is none: Rutfors is directed to an portable radio antenna device that minimizes coupling between transmit and receive antennas, and never mentions the occurrence of ESD events or issues relating to ESD protection.

Claims 2-3 and 5-8 depend from claim 1, and are allowable for at least the same reasons set forth above with respect to claim 1.

Claim 6 is also separately allowable for at least the following additional reasons. Claim 6 recites that the low voltage supply floats during the radio frequency input to high voltage supply positive discharge pulse and the radio frequency input to high voltage supply negative discharge pulse. In rejecting claim 6, the Examiner states that "Jenkins et al. in view of Duclos and Rutfors et al., *in Figure 3*, discloses the low noise amplifier [of claim 6]" (emphasis added). Applicants responded previously to this rejection by pointing out that Jenkins' Fig. 3 shows that Jenkins' protection circuit will not operate correctly if VSS is allowed to float: diode D6 will not conduct, and the ESD current will be discharged directly into buffer 102.

The Examiner now asserts that "the circuit of [Jenkins'] Fig. 3 is not relied upon for the rejection... Rather, Fig. 1 of Jenkins in combination with Duclos would perform the limitations of Claims 6 and 7." However, Fig. 1 of Jenkins does not cure this deficiency, because Fig. 1 does not include any path between the input and high voltage supply to permit a radio frequency input to high voltage supply positive discharge pulse or negative discharge pulse. In Fig. 1, the two pairs of back-to-back diodes are coupled between the differential inputs and *VSS*, the negative supply. (Col. 2, lines 47-54; col. 3, 16-21). The Examiner's proposed modification of

Jenkins to include Duclos' clamp does not supply this missing path, because Duclos' clamp would be incorporated "between the terminals of VDD and VSS" – not between the input and VDD.

Additionally, Jenkins' low voltage supply VDD cannot be allowed to merely float during ESD events – VDD and VSS are used to bias the buffer 102, and VSS must be biased to a voltage that is less than VDD (generally, at 0V). (Col. 2, lines 47-54). For at least these reasons, Applicants respectfully assert that claim 6 is separately allowable.

Claim 7 is also separately allowable for at least the following additional reasons. Claim 7 recites that the high voltage supply floats during the radio frequency input to low voltage supply positive discharge pulse and the radio frequency input to low voltage supply negative discharge pulse. As discussed above, however, Jenkins uses positive supply VDD and negative supply VSS to bias the buffer 102. (Col. 2, lines 47-54). VDD must be biased to a voltage that is greater than VSS – generally, to about 1V – and cannot be allowed to merely float during ESD events. (Col. 2, lines 49-54). The Examiner's proposed modification of Jenkins to include Duclos' clamp does not cure this deficiency: it provides a maximum that the voltage differential may not exceed, but it does not preserve the biasing conditions for the buffer's proper operation. For at least these reasons, Applicants respectfully assert that claim 7 is separately allowable.

b. Claim 9 and its dependent claims

Claim 9 is directed to a low noise amplifier that includes receiving means for receiving an RF input and shunting means to shunt ESD current during positive and negative ESD events away from the receiving means and through a first supply. The shunting means includes a pair of diode means and a separate clamping means directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an ESD event. The first diode means of the pair has a first terminal coupled to the receiving means and a second terminal directly coupled to a first supply. The second diode means of the pair has a second terminal coupled to the receiving means and a first terminal directly coupled to the first supply.

Claim 9 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 10-11 and 13-17 depend from claim 9 and are allowable for at least the same reasons set forth above with respect to claim 9.

Claim 13 is also separately allowable for at least the same reasons set forth above with respect to claim 5.

Claim 14 is also separately allowable for at least the same reasons set forth above with respect to claim 6.

Claim 15 is also separately allowable for at least the same reasons set forth above with respect to claim 7.

Claim 16 is also separately allowable for at least the same reasons set forth above with respect to claim 8.

c. Claim 17 and its dependent claims

Claim 17 is directed to an ESD protection circuit to shunt ESD current during positive and negative ESD events. The protection circuit includes a pair of diodes and a separate ESD clamp directly coupled between a high voltage supply and a low voltage supply so as to provide a discharge path there between during an ESD event. The first diode of the pair has a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply. The second diode of the pair has a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply.

Claim 17 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 18-19 and 21-23 depend from claim 17 and are allowable for at least the same reasons set forth above with respect to claim 17.

Claim 21 is also separately allowable for at least the same reasons set forth above with respect to claim 5.

Claim 22 is also separately allowable for at least the same reasons set forth above with respect to claim 6.

Claim 23 is also separately allowable for at least the same reasons set forth above with respect to claim 7.

d. Claim 24 and its dependent claims

Claim 24 is directed to an ESD protection circuit that includes shunting means for shunting ESD current during positive and negative ESD events and a separate clamping means directly coupled between a high voltage supply and a low voltage supply so as to provide a

discharge path there between during an ESD event. The shunting means includes a pair of diode means. The first diode means of the pair has a first terminal coupled to an input/output pad and a second terminal directly coupled to a first supply. The second diode means of the pair has a second terminal coupled to the input/output pad and a first terminal directly coupled to the first supply.

Claim 24 is allowable for at least the same reasons set forth above with respect to claim 1.

Claims 25-26 and 28-30 depend from claim 24 and are allowable for at least the same reasons set forth above with respect to claim 24.

Claim 28 is also separately allowable for at least the same reasons set forth above with respect to claim 5.

Claim 29 is also separately allowable for at least the same reasons set forth above with respect to claim 6.

Claim 30 is also separately allowable for at least the same reasons set forth above with respect to claim 7.

e. Claim 31 and its dependent claims

Claim 31 is directed to a method for discharging ESD that includes providing a first direct discharge path between an input/output pad and a first supply, providing a second direct discharge path between the input/output pad and the first supply, providing a third discharge path between the first supply and a second supply during an ESD event; and shunting ESD current during positive and negative ESD events through one of the first discharge path and the second discharge path.

The Examiner suggests that Jenkins' Fig. 3 shows Applicants' claimed steps of providing first and second direct paths between an input and a first supply, and shunting ESD current during positive and negative ESD events through one of the first discharge path and the second discharge path. The Examiner acknowledges that Jenkins does not teach providing a third discharge path between the first supply and a second supply during an electrostatic discharge event. The Examiner suggests that Duclos' ESD clamp in Fig. 2 meets this limitation. The Examiner further suggests that it would have been obvious to incorporate Duclos' ESD clamp

into Jenkins' design "for the purpose of providing bidirectional protection to the buffer (102) from ESD occurring from the power supply."

As discussed above with respect to claim 1, the Examiner has not carried his burden of establishing a *prima facie* case of obviousness. Jenkins already discloses a protection circuit for protecting the buffer from ESD events occurring at the supply, and this disclosed protection circuit uses a clamp configuration. Modifying Jenkins to include Duclos' clamp would be redundant in view of this existing protection. Applicants respectfully assert that claim 31 is allowable for at least these reasons.

Claims 32 and 34-36 depend from claim 31 and are allowable for at least the same reasons set forth above with respect to claim 31.

Claim 34 is also separately allowable for at least the same reasons set forth above with respect to claim 5.

Claim 35 is also separately allowable for at least the same reasons set forth above with respect to claim 6.

Claim 36 is also separately allowable for at least the same reasons set forth above with respect to claim 7.

II. Conclusion

No fees are believed to be due at this time. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

Date: 6/25/07

Mark D. Kirkland
Reg. No. 40,048

PTO Customer No. 26200
Fish & Richardson P.C.
Telephone: (650) 839-5070
Facsimile: (650) 839-5071